In the Abstract:

Please replace the existing abstract with the following new abstract:

A processor includes a series of predicate registers 135. Each predicate register is switchable between at least respective first and second states and each is assignable to one or more predicated-execution instructions. A control information holding unit 131 holds items of control information which correspond respectively to the predicate registers. An operating unit 133 is provided for each one of the predicate registers and receives items of control information $L_i$ and $L_{i+1}$ and items of state information $P_i$, $P_{i-1}$. Each operating unit is operable to perform a selected state determining operation in which the state of its own predicate register is determined in dependence upon the received items. The operating units operate in parallel with one another to perform respective such state determining operations. The state determining operations can be used to bring about state changes required in prologue, kernel and epilogue stages of a software-pipelined loop.

[Fig. 14]